Data Sheet August 2000 File Number 2928.3

Radiation Hardened 8K x 8 SOS CMOS Static RAM

The Intersil HS-65647RH is a fully asynchronous 8K x 8 radiation hardened static RAM. This RAM is fabricated using the Intersil 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95823. A "hot-link" is provided on our homepage for downloading. www.intersil.com/spacedefense/space.asp

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962F9582301QXC	HS1-65647RH-8	-55 to 125
5962F9582301QYC	HS-965647RH-8	-55 to 125
5962F9582301VXC	HS1-65647RH-Q	-55 to 125
5962F9582301VYC	HS9-65647RH-Q	-55 to 125
HS1-65647RH/PROTO	HS1-65647RH/PROTO	-55 to 125
HS9-65647RH/PROTO	HS9-65647RH/PROTO	-55 to 125

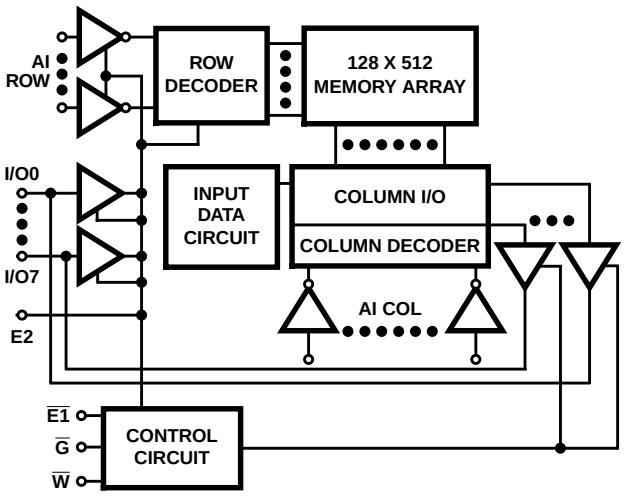
TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	MODE
X	0	X	X	Low Power Standby
1	1	X	X	Disabled
0	1	1	1	Enabled
0	1	0	1	Read
0	1	X	0	Write

Features

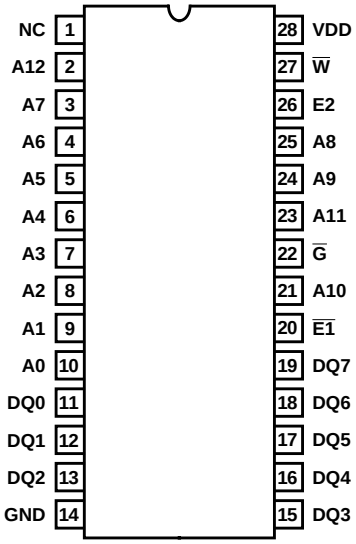
- Electrically Screened to SMD # 5962-95823
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose . . . . . 300 krad(Si) (Max)
  - Transient Upset . . . . . >1 x 10^{11} rad(Si)/s
  - Single Event Upset . . . . . < 1 x 10^{-12} Errors/Bit-Day
- Latch-up Free
- LET Threshold . . . . . >250 MEV/mg/cm2
- Low Standby Supply Current . . . . . 10mA (Max)
- Low Operating Supply Current 100mA (2MHz)
- Fast Access Time . . . . . 50ns (Max), 35ns (Typ)
- High Output Drive Capability
- Gated Input Buffers (Gated by E2)
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range . . . . . -55^{o}C to 125^{o}C
- Industry Standard JEDEC Pinout

Functional Diagram

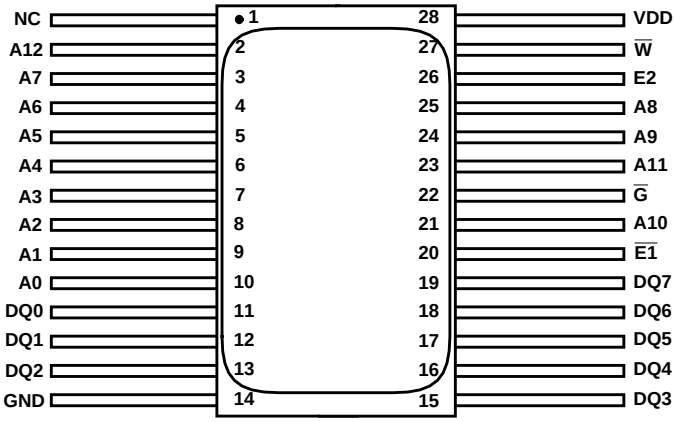


Pinout

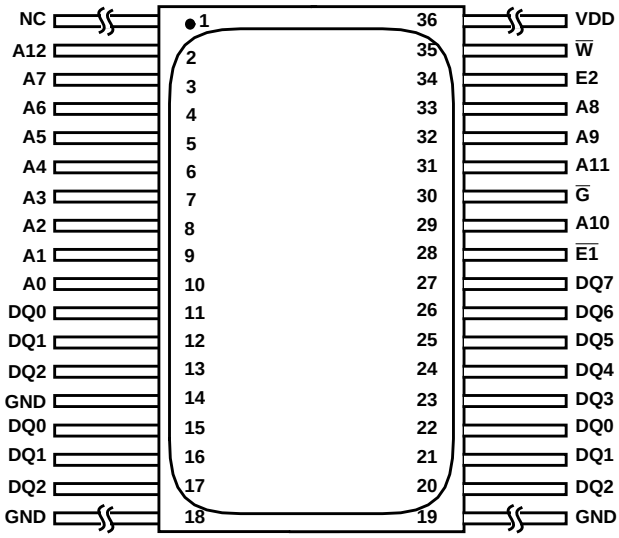
HS1-65647RH 28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T28
TOP VIEW



HS9-65647RH 28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP3-F28
TOP VIEW



HS9A-65647RH 36 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) INTERSIL OUTLINE K36.A
TOP VIEW



Timing Waveforms

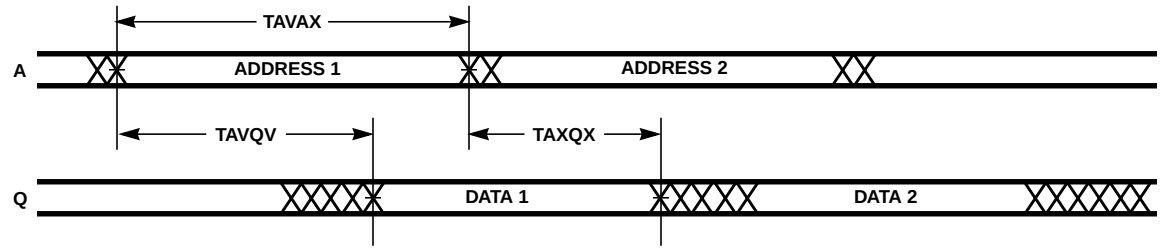


FIGURE 1. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

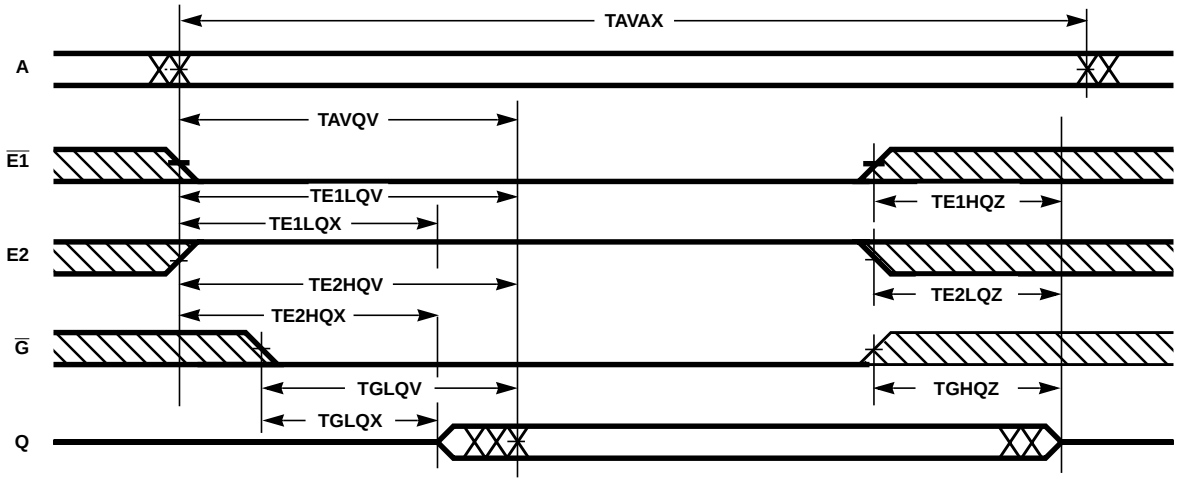


FIGURE 2. READ CYCLE II: $\overline{W}$ HIGH

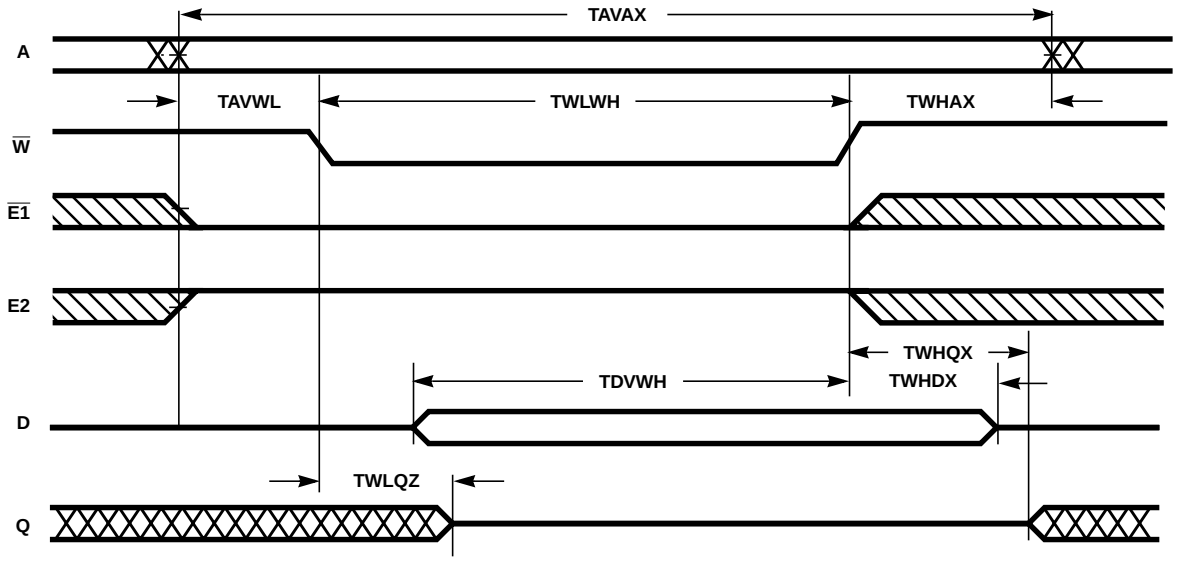


FIGURE 3. WRITE CYCLE I: LATE WRITE

Timing Waveforms (Continued)

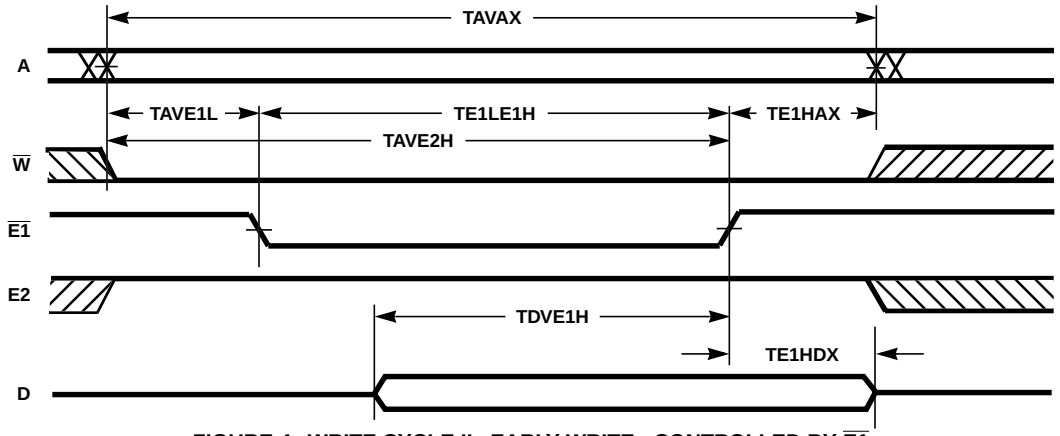


FIGURE 4. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

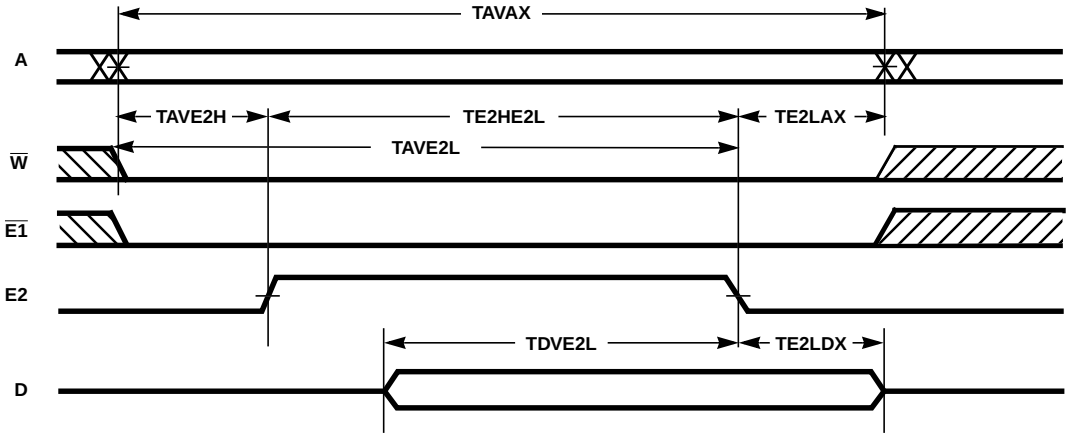


FIGURE 5. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

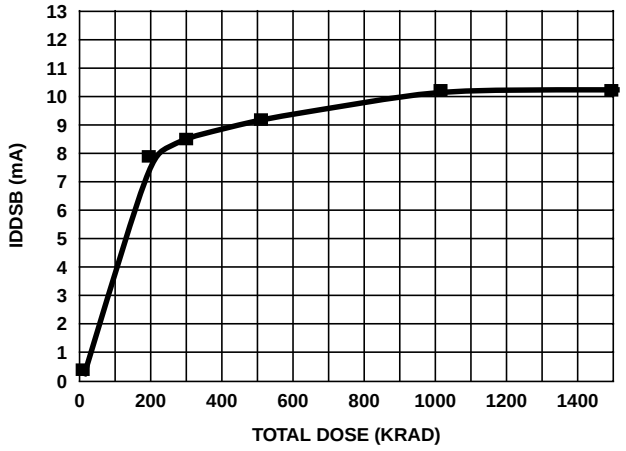


FIGURE 6.

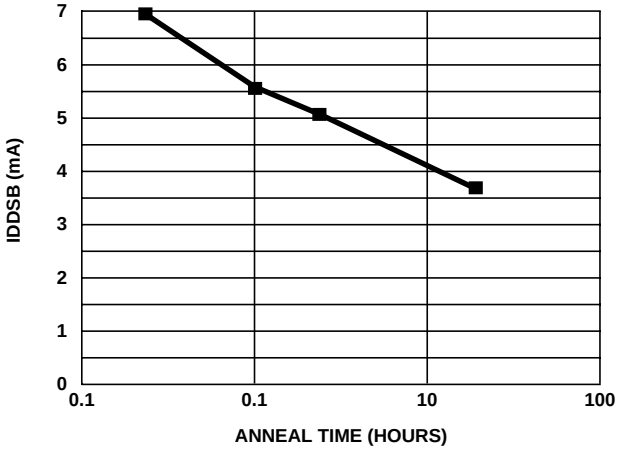


FIGURE 7.

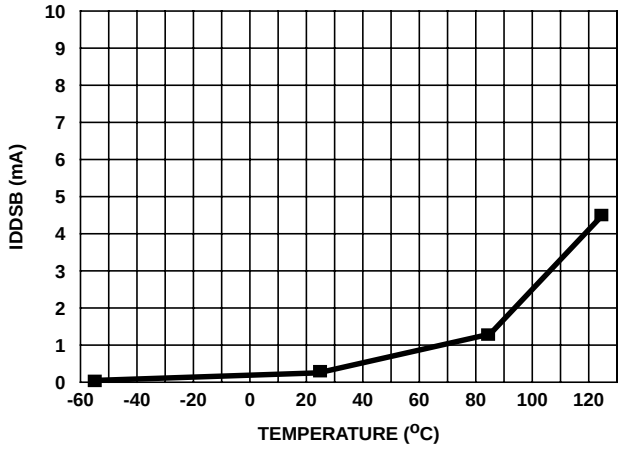


FIGURE 8.

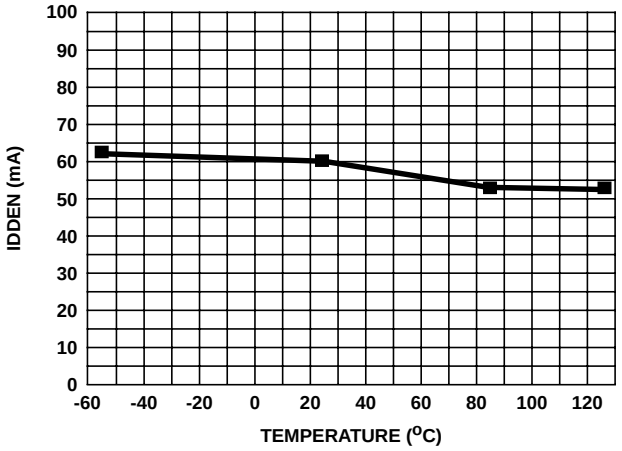


FIGURE 9.

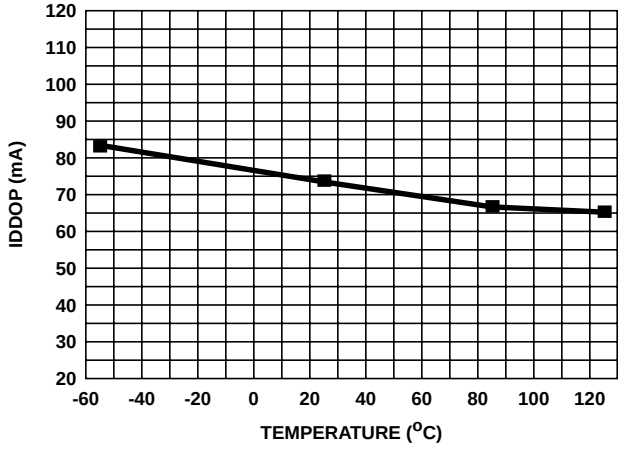


FIGURE 10.

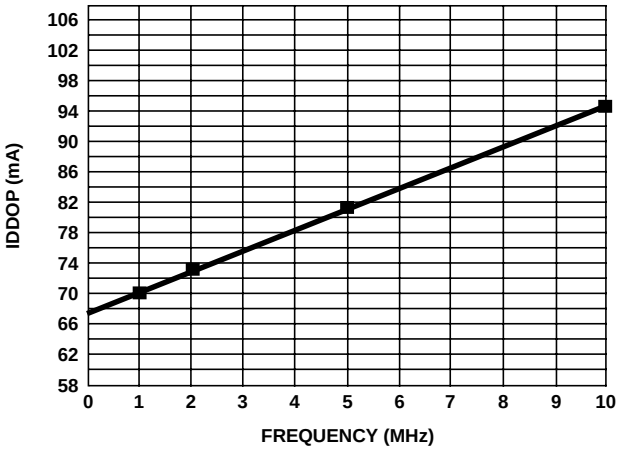
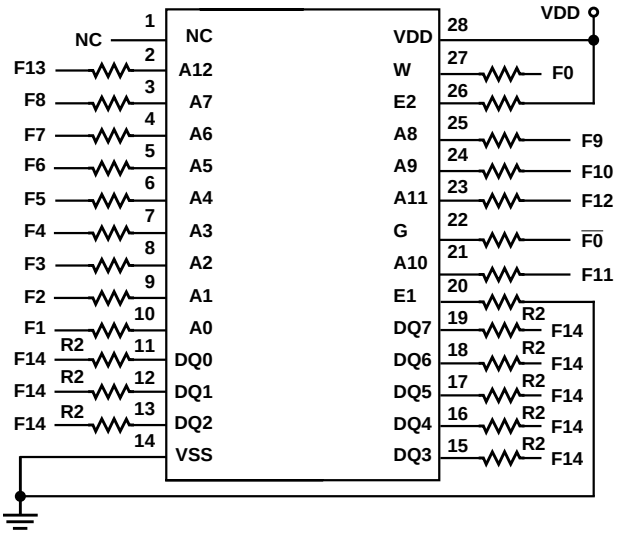


FIGURE 11.

Burn-In Circuits

HS-65647RH 28 LEAD FLATPACK AND CERAMIC DIP

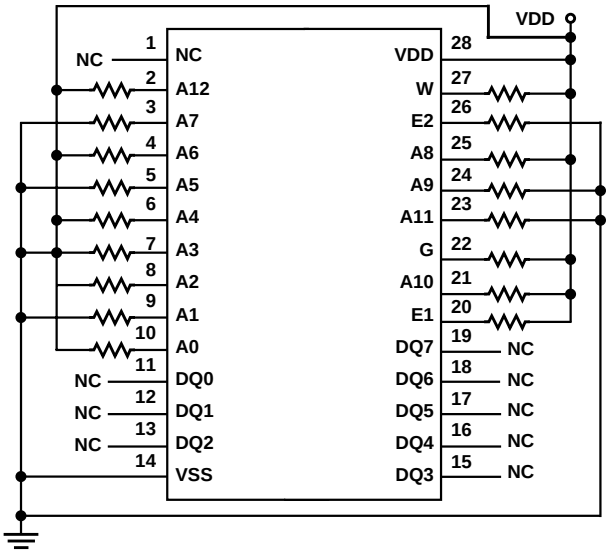


DYNAMIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min.
2. R = 10kΩ ±10%, except R2 = 47kΩ ±10%.
3. VIH: VDD ±0.5V, VIL: 0.4V ±0.4V.
4. F0 = 100kHz ±10%, 50% Duty Cycle.
5. F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2.
6. $\overline{F0}$ = inverted F0.

HS-65647RH 28 LEAD FLATPACK AND CERAMIC DIP

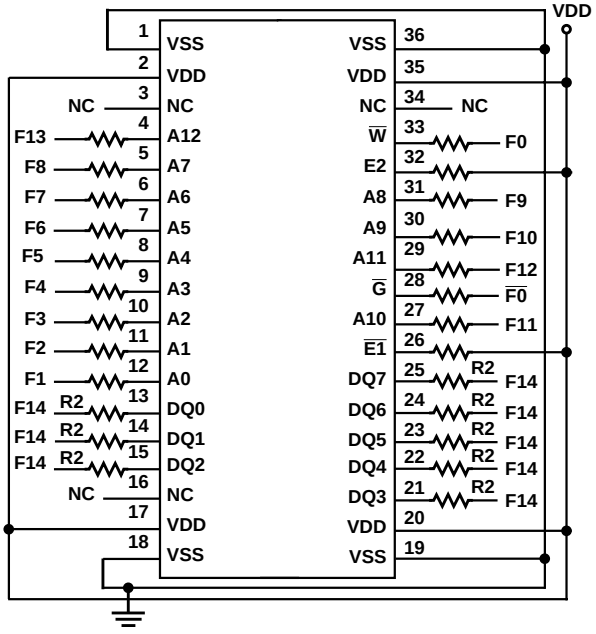


STATIC CONFIGURATION

NOTES:

7. VDD = 5.5V Min.
8. R = 10kΩ ±10%.

HS-65647RH 36 LEAD FLATPACK

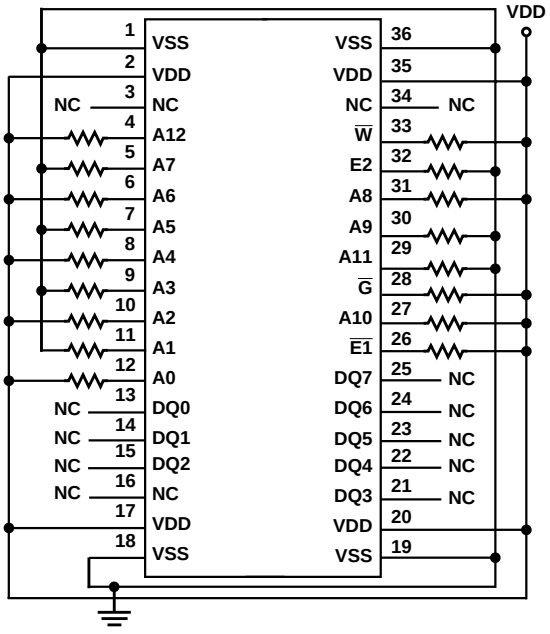


DYNAMIC CONFIGURATION

NOTES:

9. VDD = 5.5V Min.
10. R = 10kΩ ±10%, except R2 = 4.7kΩ ±10%.
11. VIH: VDD ±0.5V, VIL: 0.4V ±0.4V.
12. F0 = 100kHz ±10%, 50% Duty Cycle.
13. F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2.
14. $\overline{F0}$ = Inverted F0.

HS-65647RH 36 LEAD FLATPACK



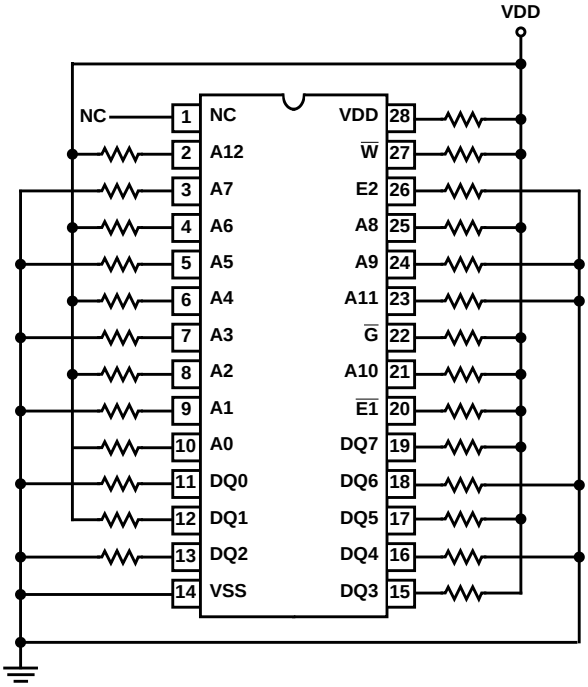
STATIC CONFIGURATION

NOTES:

15. VDD = 5.5V Min.
16. R = 10kΩ ±10%.

Irradiation Circuit

HS-65647RH (8K x 8 TSOS4 SRAM) 28 LEAD CERAMIC DIP



NOTES:

17. VDD = 5.5V ±0.5V R = 10kΩ ±10%.
18. Group E sample size is two die/wafer.

Test Patterns

MARCH (II) PATTERN

After a background of zeros is written, each cell (from beginning to end in sequence) is read, written to a one and reread. When the array is full of ones each cell (from the end to the beginning) is read, restored to a zero and reread.

After this the pattern is repeated but with complemented data.

MASEST PATTERN (Multiple Address Select Pattern)

A checkerboard pattern is written into the memory. Then the first cell is read, then its binary address complement is read. The second cell is read and then its binary address complement is read. This pattern of incrementing the address and then reading its binary address complement is repeated until the entire memory is read.

This is then repeated but using a checkerboard bar pattern.

GALROW PATTERN (Row Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the row. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

GALCOL PATTERN (Column Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the column. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

CHECKERBOARD PATTERN and CHECKERBOARD BAR

A checkerboard is written (101010) into the memory and then the pattern is read back. This is then repeated but using complemented data.

Metallization Topology

DIE DIMENSIONS:

313 mils x 291 mils x 21 mils ±1mil

METALLIZATION:

Type: Al/Si/Cu
Metal 1 Thickness: 7500Å ±2kÅ
Metal 2 Thickness: 10kÅ ±2kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.5×10^5 A/cm^2

Metallization Mask Layout

HS-65647RH